(once amended) 21. An article comprising: a storage medium, said storage medium having instructions stored thereon, said instructions, when executed, resulting in the capability to design the layout of an integrated circuit chip for fabrication, the integrated circuit chip including a gate array architecture, the gate array architecture comprising a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites to form N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors[.];

successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions; and

immediately successive rows within similarly-sized diffusion regions have opposite polarity.

REMARKS

The above-referenced continued prosecution application (hereinafter "application") has been reviewed in light of the Final Office Action, dated April 26, 2000, and the Advisory Action, dated June 29, 2000, in which: claims 1-12 and 21-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran et al. (U.S. Patent 5,780,883); and claims 1-12 and 21-26 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato (U.S. Patent 4,816,887). Consideration of the application in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-11 and 21-26 are pending the application. Claim 12 has been canceled. No new claims have been added. Claims 1 and 21 have been amended.

The Examiner has rejected claims 1-12 and 21-26 under 35 U.S.C. § 103(a) as being unpatentable over Tran. This rejection by the Examiner is respectfully traversed.

In response to Applicant's arguments in the previous response, mailed on March 28, 2000, that Tran does not disclose partially overlying polysilicon landing sites, the Examiner states "Nothing in Tran discloses that 'the non-overlying polysilicon landing sites' as argued by the Applicants. In fact figures 3A and 3B show the polysilicon gates 54 overlying the regions 42, 44, 46 and 48." It is respectfully asserted that these assertions by the Examiner incorrectly represent Applicant's arguments and, therefore, do not render the invention as recited in claim 1, for example, obvious.

In this regard, as Applicant specifically asserted in the previous response, claim 1 patentably distinguishes from Tran in at least the aspect of "diffusion regions having **partially overlying polysilicon landing sites** to form N-type and P-type transistors." Therefore, **Applicant's position is that Tran does not disclose partially overlying polysilicon landing sites, not that Tran discloses non-overlying polysilicon landing sites, as asserted by the Examiner.** Regardless of this characterization of Applicant's argument, the Examiner's reference to the figures of Tran is still unavailing as it is respectfully asserted that Tran does not render claim 1, for example, obvious. In this respect, though the invention is not limited to any particular embodiment, comparing FIG. 1 of the application with FIGs. 3A and 3B of the cited patent is illustrative of this point. FIG. 1 of the application illustrates that each "partially overlying" polysilicon landing sites overlies similarly sized N-diffusion and P-diffusion regions to form both a N-type transistor and a P-type transistor. In contrast, FIGs. 3A and 3B of Tran illustrates non-overlying polysilicon landing sites that extend over only N-diffusion or P-diffusion. That is, **the non-overlying polysilicon landing sites in Tran form either a N-type transistor or a P-type transistor, while the partially overlying polysilicon landing sites, such as in FIG. 1 of the application, form similarly sized N-type and P-type transistors.**

While Applicant respectfully asserts that the foregoing is sufficient to overcome the Examiner's rejection, in order to further prosecution, Applicant has canceled claim 12 and incorporated the limitations of that claim in claim 1 of the application to further distinguish this claim from the cited patent. The other independent claim, 21, has been similarly amended to also include the limitations of claim 12. Applicant, however, respectfully reserves the right to pursue the original claim language on any subsequent appeal. In this regard, claim 1, as amended, for example, now specifically recites:

> An integrated circuit comprising: a gate array architecture;
> said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions;
> said diffusion regions having partially overlying polysilicon landing sites to form N-type and P-type transistors;
> wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors;
> successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions; and
> immediately successive rows within similarly-sized diffusion regions have opposite polarity.

As one example of how this amendment further distinguishes claim 1 from the cited patent, claim 1, as amended, now states, in part, that "successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions." Examining the Tran patent demonstrates that **Tran does not disclose that "successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions. The "regular sized" diffusion regions in Tran are not successive.** In this regard, as was discussed in Applicant's previous response, Tran is disadvantageous as its configuration would require additional design complexity and not realize the potential power advantages of embodiments in accordance with, for example, claim 1, as amended.

Based on the foregoing, it is respectfully asserted that Tran would not render claim 1, as amended, obvious to one of ordinary skill in the art. Specifically, one of ordinary skill having this patent before him or her would be unable to produce the invention as recited in claim 1, as amended, for at least the reasons discussed above. Therefore, it is respectfully requested that the Examiner withdraw his rejection.

Claims 2-11 depend from and include all the limitations of claim 1, as amended. Therefore, it is respectfully asserted that these claims distinguish from the cited patent on the same basis as claim 1, as amended. It is respectfully requested that the Examiner withdraw his rejection of claims 2-11.

The Examiner has also rejected claim 21 under 35 U.S.C. § 103(a) on Tran. Without addressing the merits of the Examiner's comments regarding claim 21, which are, therefore, not conceded, Applicant respectfully points out that claim 21, as amended, contains similar limitations to those discussed above with respect to claim 1, as amended. Therefore, it is respectfully asserted that claim 21, as amended, patently distinguishes from Tran for similar reasons as discussed above regarding claim 1, as amended. It is respectfully requested that the Examiner withdraw his rejection.

Claims 22-26 depend from and include all the limitations of claim 21, as amended. Therefore, it is respectfully asserted that these claims distinguish from the cited patent on the same basis as claim 21, as amended. It is respectfully requested that the Examiner withdraw his rejection of claims 22-26.

The Examiner has rejected claims 1-12 and 21-26 under 35 U.S.C. § 103(a) as being unpatentable over Sato. This rejection by the Examiner is respectfully traversed.

As was asserted in Applicant's previous response, Applicant believes that the Examiner's rejection is procedurally insufficient under MPEP § 706 as the Examiner has not

"clearly articulate[d] [the] rejection early in the prosecution process." In this respect, the Examiner stated in the Office Action, mailed on December 30, 1999, that "Sato discloses a gate array having two distinct transistor sizes on the order of one-third. It would have been obvious that Sato discloses the claimed device." In response to Applicant's arguments in the previous response the Examiner merely states that "Figure 8 of Sato also show the polysilicon gates 7G1, 7G2, 10G1, 10G2, and 3G1 overlying the diffusion regions." Examination of these elements of Sato's Figure 8 illustrates that this assertion by the Examiner is incorrect for, at least, reasons similar to those discussed with respect to the Examiner's rejection of claim 1 under Tran.

Notwithstanding the foregoing, and in the interest of furthering prosecution, Applicant has amended claim 1 to include the limitations of claim 12. Applicant, however, as previously noted, respectfully reserves the right to pursue the original claim language on any subsequent appeal. In this regard, Applicant respectfully asserts that **claim 1, as amended, distinguishes from Sato for, at least, reasons similar to those discussed above with respect to Tran, such as, for example, that "successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions."** Therefore, it is respectfully requested that the Examiner withdraw his rejection.

Claims 2-11 depend from and include all the limitations of claim 1, as amended. Therefore, it is respectfully asserted that these claims distinguish from the cited patent on the same basis as claim 1, as amended. It is respectfully requested that the Examiner withdraw his rejection.

The Examiner has also rejected claim 21 on the same basis as claim 1. Therefore, the arguments made regarding the procedural insufficiency of the Examiner's rejection with respect to claim 1 are relevant and apply here as well. Applicant also respectfully points out that claim 21, as amended, contains similar limitations to those discussed above with respect to claim 1, as amended. Therefore, it is respectfully asserted that claim 21, as amended, patentably distinguishes from Sato for similar reasons as discussed above regarding claim 1, as amended. It is respectfully requested that the Examiner withdraw his rejection.

Claims 22-26 depend from and include all the limitations of claim 21, as amended. Therefore, it is respectfully asserted that these claims distinguish from the cited patent on the same basis as claim 21, as amended. It is respectfully requested that the Examiner withdraw his rejection.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application, as amended, are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 264-0967. Reconsideration of this patent application and early allowance of all the claims, as amended, is respectfully requested.

Respectfully submitted,

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